Abstract

An image scaler included in or coupled to a digital display unit that optionally upscales analog display data in the form of a source image represented by source image pixel data to form a destination image represented by destination image pixel data is described. A clock generator generates a number of clock signals one or more of which may be synchronized with a time reference signal associated with the analog display data. In one embodiment, the source image pixel data is received in accordance a first clock and the image scaler generates the destination image in accordance with a second clock. The second clock is computed in relation to the first clock such that the scaler is implemented using a line buffer since a period of time to provide the source image pixel data is about equal to a period of time to provide the destination image pixel data.